

## REMARKS

Claims 1-32 are pending in the present application. Applicants thank the Examiner for allowing all pending claims.

### Objections to the drawings:

The Examiner objected to the drawings for failing to show every feature. Applicants amended Fig. 3 to more clearly show that regions 33 and 32 may overlap by a dotted line. Thus, an overlapping region is identified. Applicants submit a marked up copy of the sheet comprising Fig. 3. Furthermore, a formal set of drawings is hereby submitted.

The Examiner objected to Fig. 3 for comprising an illegible reference characters above numeral 27. The formal drawings show that there are no numerals above numeral 27. In fact, in a former version, numeral 28 used to be located above numeral 27 and has been not completely erased.

The specification has been amended to properly identify numeral 9 in Fig. 2. The source electrode is shown in Fig. 2 similarly as drain electrode 10. thus, no new matter has been added.

### Objections to the specification:

The Examiner objected to the abstract and to some informalities in the specification. Applicants amended both abstract and specification according to the Examiner's proposal.

## CONCLUSION

Applicants do not believe that any other fees are due at this time; however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be required for any reason relating to this document, the Commissioner is authorized to deduct the fees from Deposit Account No. 02-0383, (*formerly Baker & Botts, L.L.P.*,) Order Number 068736.0231.

BAKER BOTTS, L.L.P.

Date: April 6, 2005

By:

Andreas H. Grubert

(Limited recognition 37 C.F.R. §10.9)

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AGENT FOR APPLICANTS

Title: "LDMOS Transistor"  
Inventor(s): Olof Tornblad et al.  
Attorney Docket #068736.0231

Red-Lined (Amended) Sheet - Fig. 3

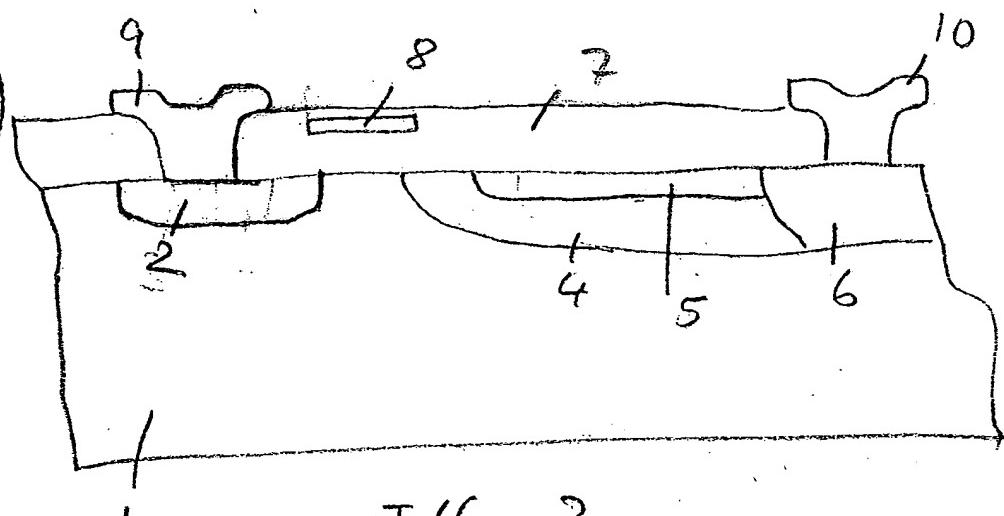


FIG. 2  
(PRIOR ART)

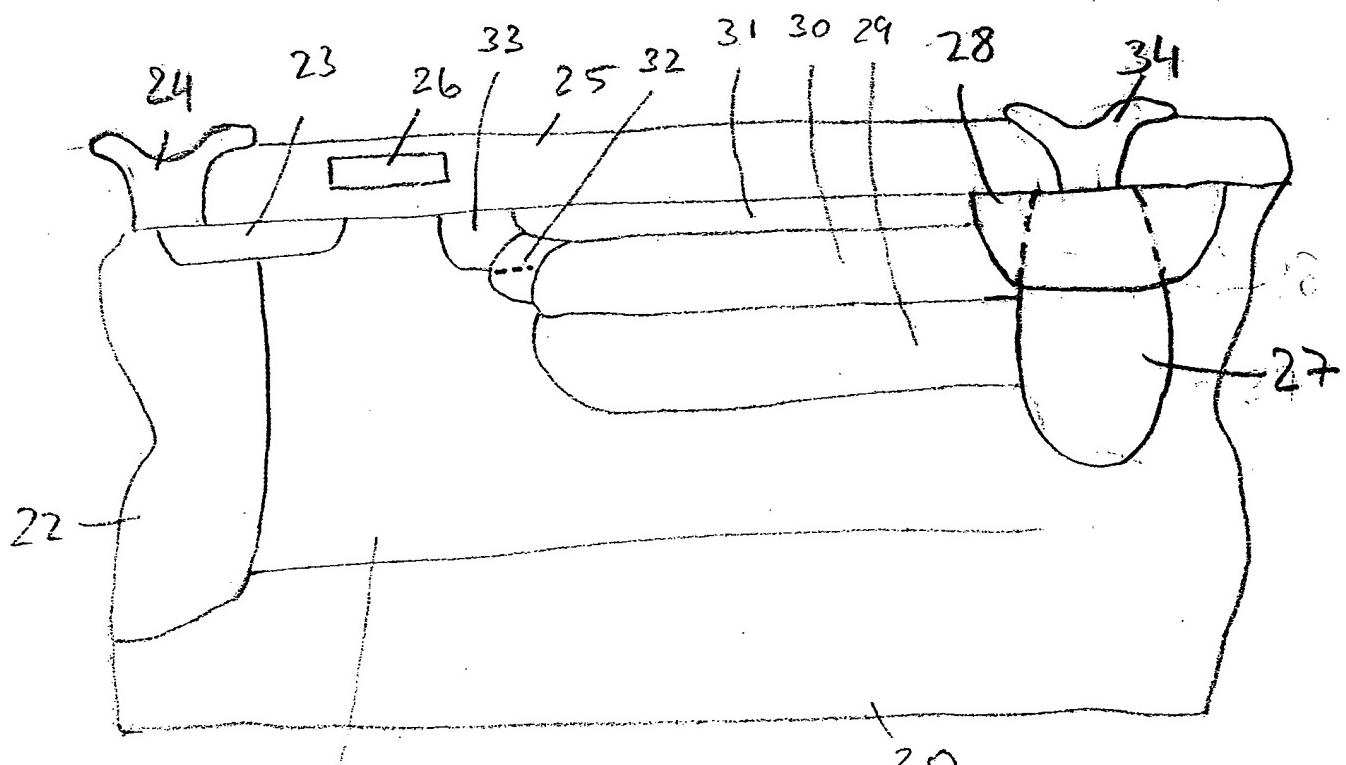


FIG. 3